



Controllable Bridgeless CUK Rectifiers for PFC Applications

Nikhil Mohanan¹, Daisykutty Abraham², Geethu James³

P.G. student, Mar Athanasius College of Engineering, Kothamangalam, Kerala, India ¹

Professor, Mar Athanasius College of Engineering, Kothamangalam, Kerala, India²

Assistant Professor, Mar Athanasius College of Engineering, Kothamangalam, Kerala, India³

ABSTRACT: Power supplies with active power factor correction (PFC) techniques are becoming necessary to meet harmonic regulations and standards. Conventional PFC scheme has lower efficiency due to significant losses in the diode bridge. In an effort to maximize the power supply efficiency, considerable research efforts have been directed toward designing bridgeless PFC circuits, where the number of semiconductors generating losses is reduced by eliminating the full bridge input diode rectifier. A bridgeless PFC Rectifier allows the current to flow through a minimum number of switching devices compared to the conventional PFC rectifier. Accordingly, the converter conduction losses can be significantly reduced and higher efficiency can be obtained, as well as cost savings. Several bridgeless topologies, which are suitable for step-up/step-down applications have been introduced. The CUK converter offers several advantages in PFC applications. Unlike the SEPIC converter, the CUK converter has both continuous input and output currents with a low current ripple. Thus, for applications which require a low current ripple at the input and output ports of the converter, the CUK converter seems to be a potential candidate in the basic converter topologies. Due to the lower conduction and switching losses, the bridgeless CUK topology can further improve the conversion efficiency when compared with the conventional CUK PFC rectifier. To maintain the same efficiency, these circuits can operate with a higher switching frequency. It will reduce the size of the PFC inductor and EMI filter. The power factor value can be achieved up to 0.9136 using this circuit with a power of 166 W. It is proven by using MATLAB simulation.

KEYWORDS: Bridgeless rectifier, CUK converter, low conduction losses, power factor correction (PFC) rectifier, total harmonic distortion (THD).

I. INTRODUCTION

Power factor (PF) is defined as the ratio of real power to apparent power, where real power produces real work and apparent power is the product of RMS value of voltage and current. When PF is not 1, the current waveform does not follow the voltage waveform. This results in power losses and may also cause harmonics that travel down the neutral line and disrupt other devices connected to the line. The power Factor Correction (PFC) circuit basically shapes the input current waveform to be the replica of the input voltage waveform and exactly in phase with it. Active PFC is preferred to passive one because of its small form factor and much better PF. Active PFC [3] is usually based on dc-dc converter where the feedback control can be performed in continuous conduction mode (CCM), discontinuous conduction mode (DCM), or critical conduction mode (CRM). Converter that operates in CCM induces small device current stress and the requirement on input filter is relaxed. However, the hard turn-OFF of freewheeling diode increases power loss and switching noise. DCM is commonly used for low-power application. However, a conventional PFC scheme has lower efficiency due to significant losses in the diode bridge. Most of the PFC Rectifiers utilize a boost converter [5] at their front end. Several bridgeless PFC Rectifiers have been introduced to improve the rectifier power density and/or reduce noise emissions via soft-switching techniques or coupled magnetic topologies. On the other hand, the bridgeless boost rectifier has the same major practical drawbacks as the conventional boost converter such as the dc output voltage is higher than the peak input voltage, lack of galvanic isolation, and high start-up inrush currents. Therefore, for low-output voltage applications, such as telecommunication or computer industry, an additional converter or an isolation transformer is required to step-down the voltage. Bridgeless buck PFC rectifier used

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in step-down applications. It has the major disadvantage of higher Total Harmonic Distortion (THD), reduced power factor and limited voltage ratio. To overcome these drawbacks CUK converter based system [1] is introduced.

The CUK converter offers several advantages in PFC applications, such as better transformer isolation, natural protection against inrush current occurring at start-up or overload current, lower input current ripple, and less electromagnetic interference (EMI) associated with the discontinuous conduction mode (DCM) topology. Unlike the SEPIC converter, the CUK converter has both continuous input and output currents with a low current ripple. Thus, for applications, which require a low current ripple at the input and output ports of the converter, the CUK converter seems to be a potential candidate in the basic converter topologies.

II. BRIDGELESS CUK RECTIFIER FED PFCS

Bridgeless CUK converter topology is formed by connecting two dc–dc CUK converters, one for each half-line period (T/2) of the input voltage. By using lesser number of semiconductor switches, the losses due to current stresses in the switches reduced and the circuit efficiency is improved compared to the conventional CUK Rectifiers.

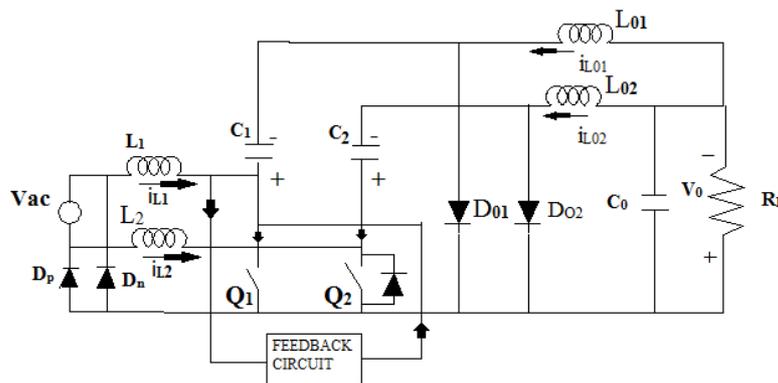


Fig. 1. Circuit diagram of Bridge less CUK converter system

Due to the symmetry of the circuit, it is sufficient to analyze the circuit during the positive half cycle of the input voltage. Moreover, the operation of the Circuit in Fig.1 will be described assuming that the three inductors are operating in DCM. The advantages of using DCM [2] includes near-unity power factor, the power switches are turned ON at zero current, and the output diodes (D_{01} and D_{02}) are turned OFF at zero current. Thus, the losses due to the turn-ON switching and the reverse recovery of the output diodes are considerably reduced. Conversely, DCM operation significantly increases the conduction losses due to the increased current stress through circuit components, which limits its use to low-power applications.

III. PRINCIPLE OF OPERATION AND ANALYSIS

A. Principle of Operation

Similar to the conventional CUK converter, the circuit operation in DCM can be divided into three distinct operating stages during one switching period T_s . Fig.2 shows the equivalent circuits and theoretical DCM waveforms over one switching cycle during the positive half cycle of the input voltage. The working over one switching cycle can be described as follows,

1) *Stage 1* [t_0-t_1]: The switch Q_1 is turned ON at t_0 . Diode D_p is forward biased by the inductor current i_{L1} . As a result, the diode D_n is reverse biased by the input voltage. The output diode D_{01} is reverse biased by the reverse voltage ($V_{ac} + V_o$), while D_{02} is reverse biased by the output voltage V_o . In this stage, the currents through inductors L_1 and L_{01} increase linearly with the input voltage, while the current through L_{02} is zero due to the constant voltage across C_2 .

2) *Stage 2* [t_1-t_2]: The switch Q_1 is turned OFF and the diode D_{01} is turned ON at t_1 simultaneously providing a path for the inductor currents i_{L1} and i_{L01} . The diode D_p remains conducting to provide a path for i_{L1} . Diode D_{02} remains reverse

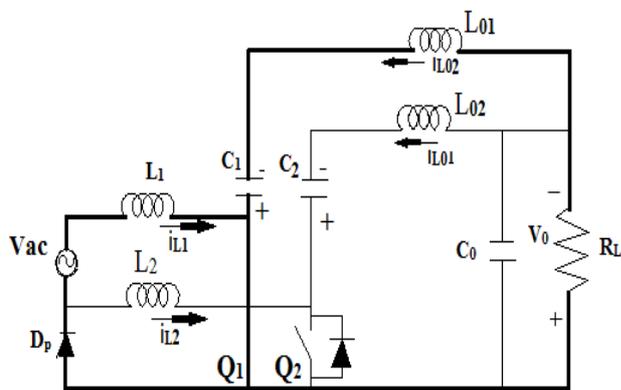
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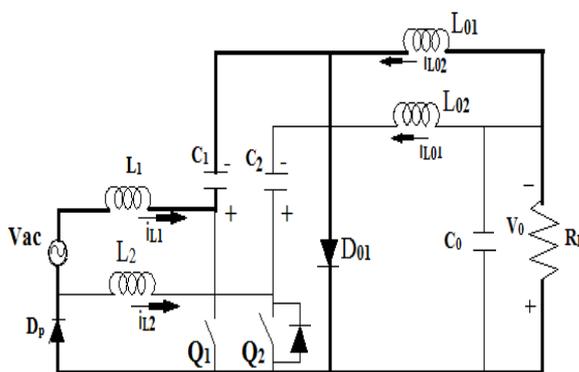
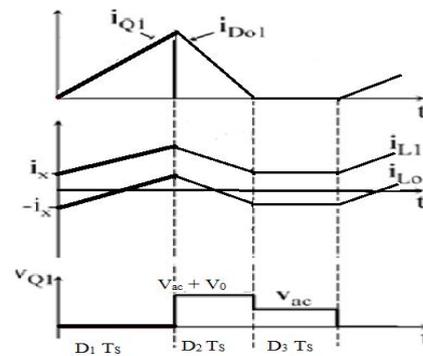
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biased during this interval. This interval ends when $i_{D_{01}}$ reaches zero and D_{01} becomes reverse biased. Diode D_{01} works with Zero current switching.

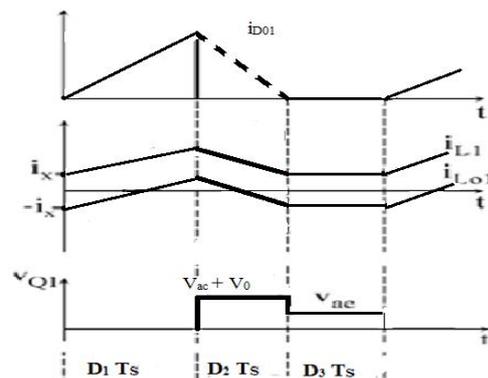
3) Stage 3 [t_2 - t_3]: During this interval, only the diode D_p conducts to provide a path for i_{L1} . Accordingly the inductors in this interval behave as constant current sources. Hence, the voltage across the three inductors is zero. The capacitor C_1 is being charged by the inductor current i_{L1} . This period ends when Q_1 is turned ON. Since the diode D_p continuously conducts throughout the entire switching period, the average voltage across C_2 is equal to the output voltage V_o . As a result, a negligible ac current will flow through C_2 and L_{o2} . Therefore, the current through L_2 during the positive half cycle of the input voltage is equal to the negative current through the body diode of Q_2 . It should be noted that the body diode of the inactive switch Q_2 is always conducting current during the positive half cycle of the input voltage. This is due to the low impedance of the input inductors (L_1 and L_2) at the line frequency.



(a)



(b)



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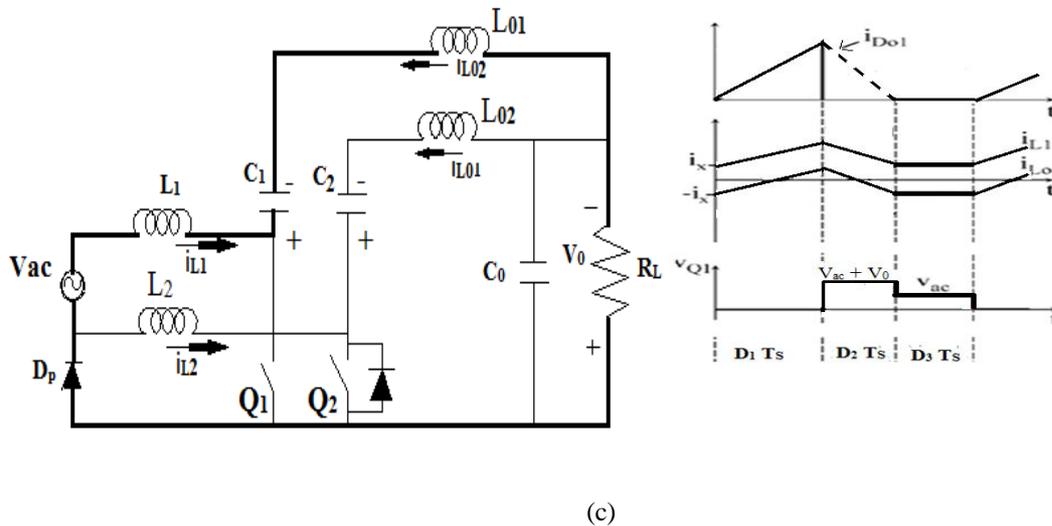


Fig. 2. Equivalent circuits and theoretical DCM waveforms during one switching period, T_s .
(a) Q_1 ON (b) Q_1 OFF and D_{01} ON (c) Q_1 and D_{01} OFF

B. Voltage Conversion Ratio.

The voltage conversion ratio M in terms of the converter parameters can be obtained by applying the power balance principle.

$$\text{Voltage Conversion Ratio, } M = \frac{V_0}{V_m} = \sqrt{\frac{R_L}{2R_e}} \quad (1)$$

Where V_0 = output voltage, V_m = peak input voltage, R_L = Load resistance.

$$R_e = \frac{2L_e}{D_1^2 T_s}, \quad L_e = \text{Effective inductance. } D_1 = \text{Duty ratio of } Q_1, \quad T_s = \text{Switching period.}$$

C. Capacitor Selection

The energy transfer capacitors C_1 and C_2 are important elements in the circuit since their values greatly influence the quality of input line current. Its values must be chosen such that their steady state voltages follow the shape of the rectified input ac line voltage waveform plus the output voltage with minimum switching voltage ripple as possible. Also, the values of C_1 and C_2 should not cause low frequency oscillations with the converter inductors. In practical design, values of C_1 and C_2 are determined based on inductors L_1 , L_0 values such that the resonant frequency (f_r) during DCM stage is higher than line frequency (f_l) and well below switching frequency (f_s). Thus,

$$f_l < f_r < f_s \quad \text{Where } f_r = \frac{1}{2\pi\sqrt{C_1(L_1+L_0)}}$$

Output capacitor C_0 needs to be sufficiently large to store minimum energy required for balancing the difference between the time varying input power and constant load power.

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IV. SIMULINK MODEL

A. Simulink Models

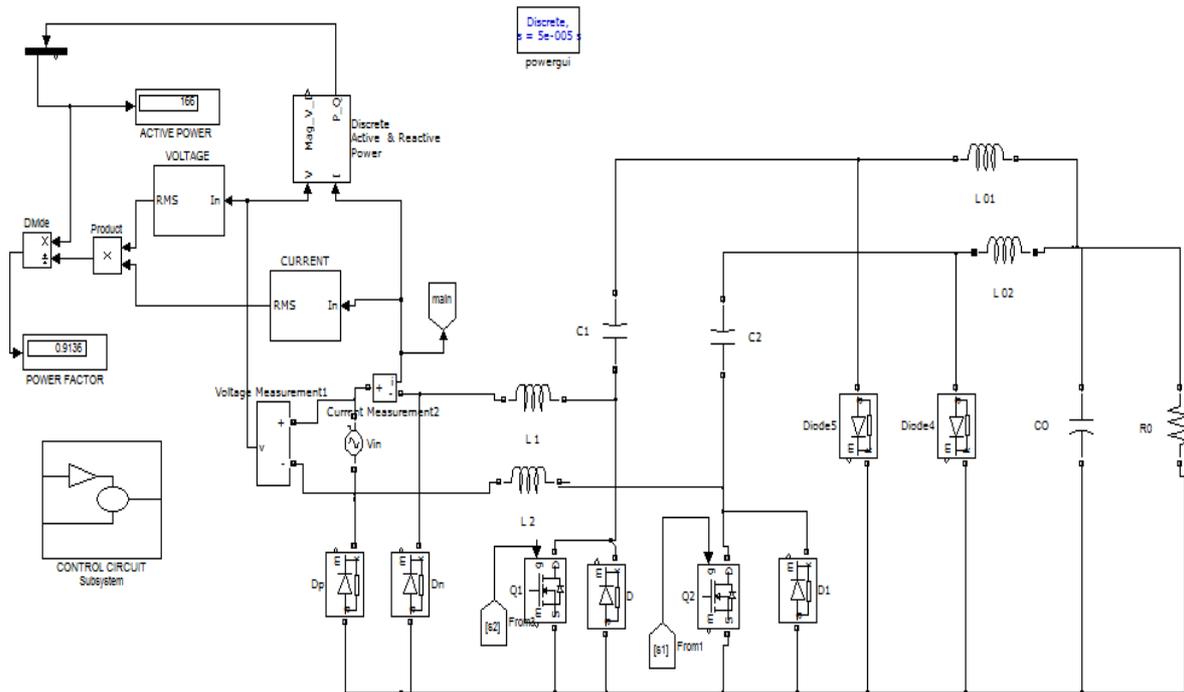


Fig. 4. Simulink model of Bridgeless CUK converter system with feedback.

The performance analysis of Controllable bridgeless CUK converter done by evaluating simulation waveforms. The tool used was MATLAB SIMULINK. Fig. 6(a), 6(b), 6(c), 6(d) shows the simulation wave forms of input voltage and current, output voltage and input inductor current, gate signals to Q_1 and Q_2 respectively.

Simulation parameters are given below

- a) Input Inductor : 25 mH
- b) Output inductor : 1 μ H
- c) Output capacitance : 22000 μ F
- d) Energy transfer capacitor : 150 μ F
- e) Input voltage : 100 V AC

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B. Control Circuit

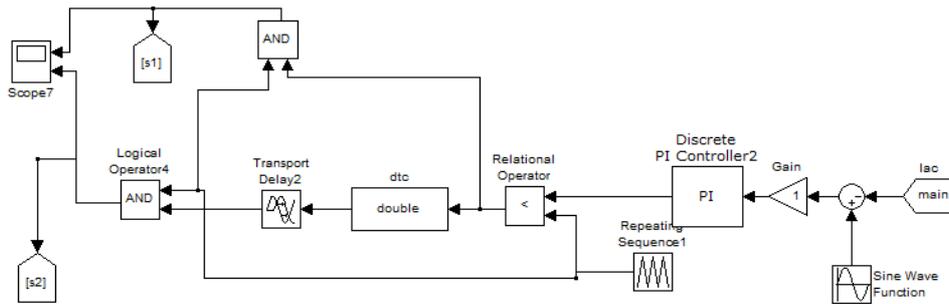
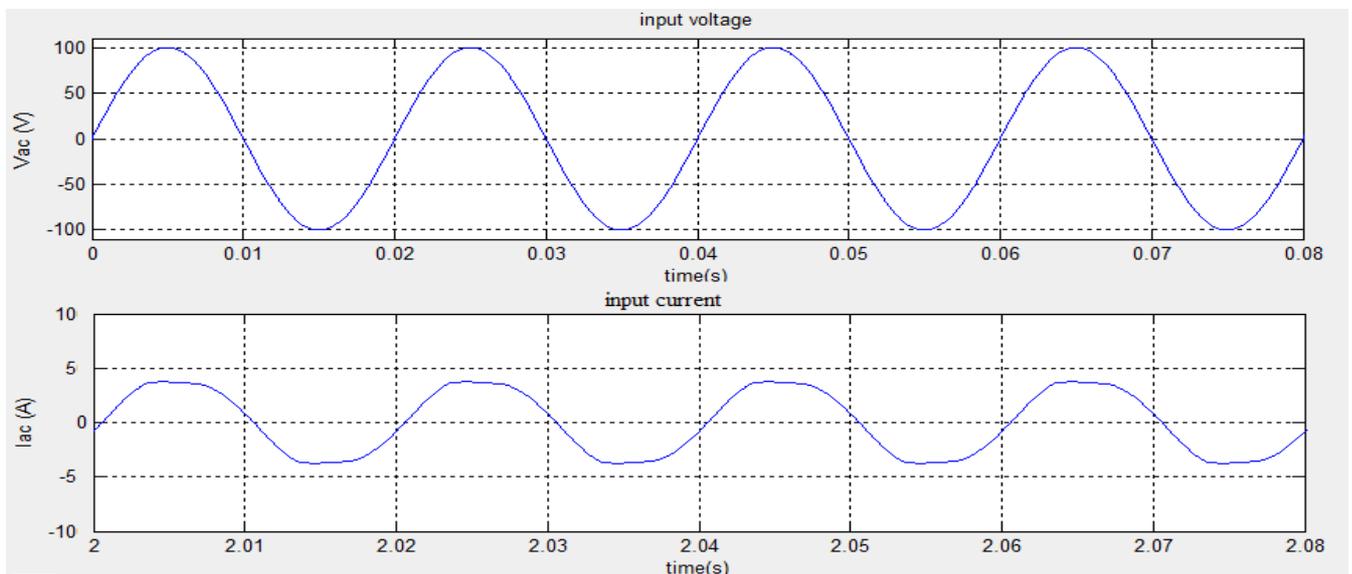


Fig. 5. Control circuit.

The feedback loop works with Sinusoidal Pulse Width Modulation (SPWM). Gate signals for Q1 and Q2 produced by the control circuit given in Fig. 5. Gate signals are proportional to the deviation of input current waveform from the desired shape. Input current wave form is compared with a desired sinusoidal signal. Difference of both signals (error signal) given as the input of PI (Proportional-Integral) controller. PI controller's output compared with a triangular waveform of desired switching frequency. Output of relational operator provides the gate pulses.

V. SIMULATION RESULTS



(a)

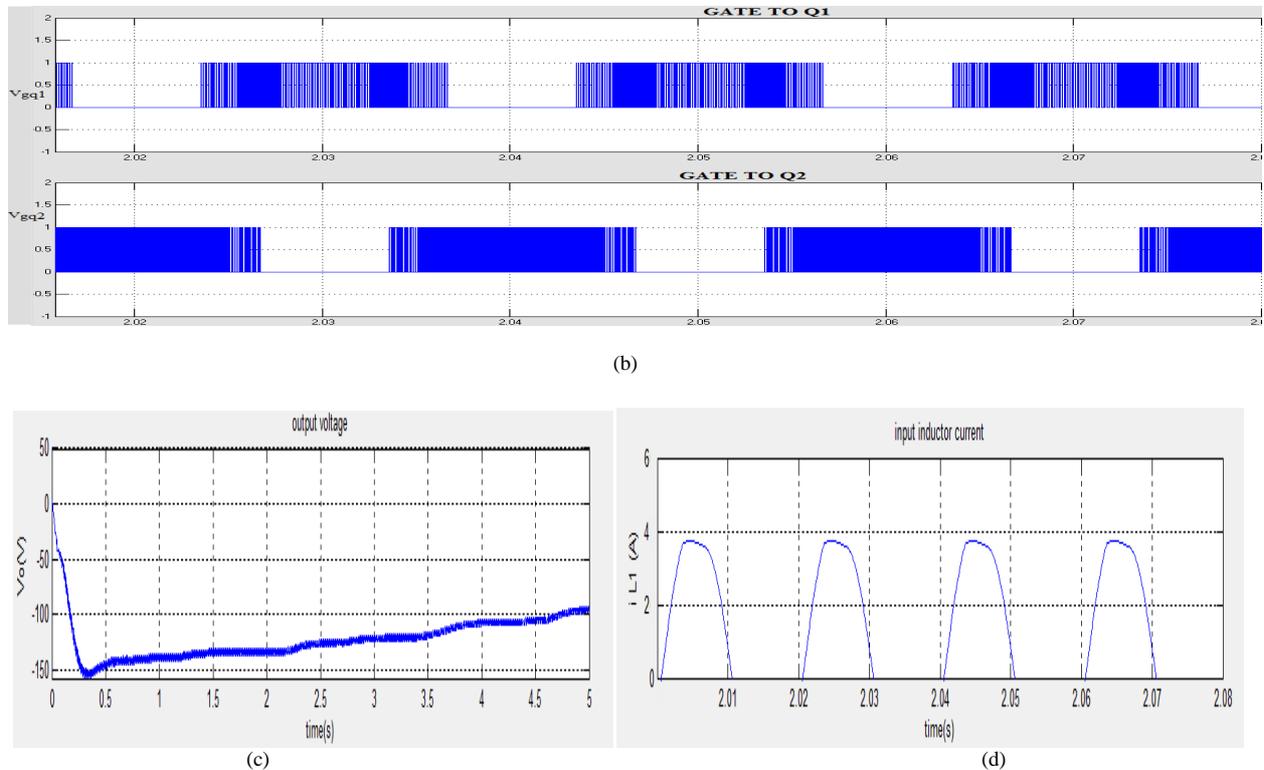


Fig 6. Simulation results (a) Input voltage and current (b) gate signals (c) Output voltage (d) Input inductor current

From simulation results we can understand that input current and voltage are in phase. So Power factor is nearly unity. Using this circuit we can improve the power factor up to 0.9136 with a power of 166 watts.

VI. COMPARISON STUDY

The Bridge less CUK converter circuit has higher component count, but lower current stresses [6][7]. The converter chooses according to the application. Efficiency of this circuit is higher than that of the conventional PFC CUK Rectifier for the provided output power levels due to lesser number of switches in conduction path. As the power level increases it shows some drawbacks. In this case, it is preferred to operate the converter in CCM region instead of DCM. Its THD value is less than 2%. For lower power levels they are designed to operate in DCM. DCM offers several advantages. With the introduction of closed loop control it become more stable with better Power Factor. Power factor improved from 0.9 to 0.916. Small and Simple control circuit is provided.

VII. CONCLUSION

Single –phase ac-dc bridgeless rectifier based on CUK topology are presented and discussed in this paper. The performance of the Bridgeless CUK converter topology is verified by simulation. Due to the lower conduction and switching losses, this topology can further improve the conversion efficiency compared to conventional system. To maintain the same efficiency, these circuits can operate with a higher switching frequency which helps to use small size filter components. It can possess low THD value less than 2%. It can work with near unity power factor.

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